

# DEVICE THRESHOLD CONTROL OF FRONT-GATE SILICON-ON-INSULATOR MOSFET USING A SELF-ALIGNED BACK-GATE

## ABSTRACT OF THE DISCLOSURE

The present invention provides SOI CMOS technology whereby a polysilicon back-gate is used to control the threshold voltage of the front-gate device, and the nMOS and pMOS back-gates are switched independently of each other and the front gates. Specifically, the present invention provides a method of fabricating a back-gated fully depleted CMOS device in which the device's back-gate is self-aligned to the device's front-gate as well as the source/drain extension. Such a structure minimizes the capacitance, while enhancing the device and circuit performance. The back-gated fully depleted CMOS device of the present invention is fabricated using existing SIMOX (separation by ion implantation of oxygen) or bonded SOI wafers, wafer bonding and thinning, polySi etching, low-pressure chemical vapor deposition and chemical-mechanical polishing.